

Fig. 1 A

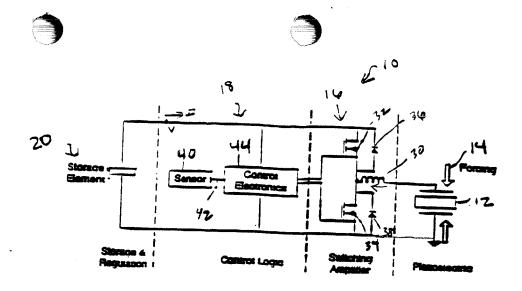


Fig. 1B

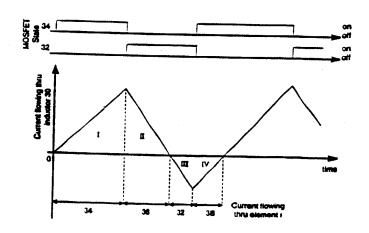
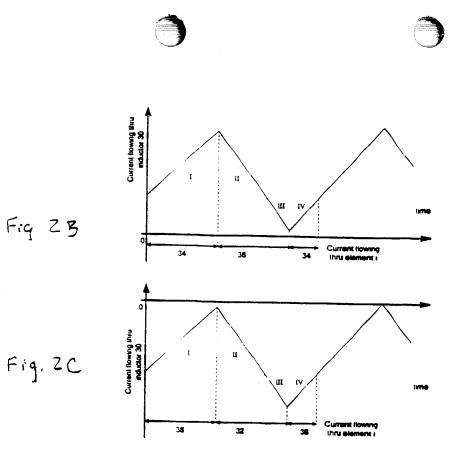
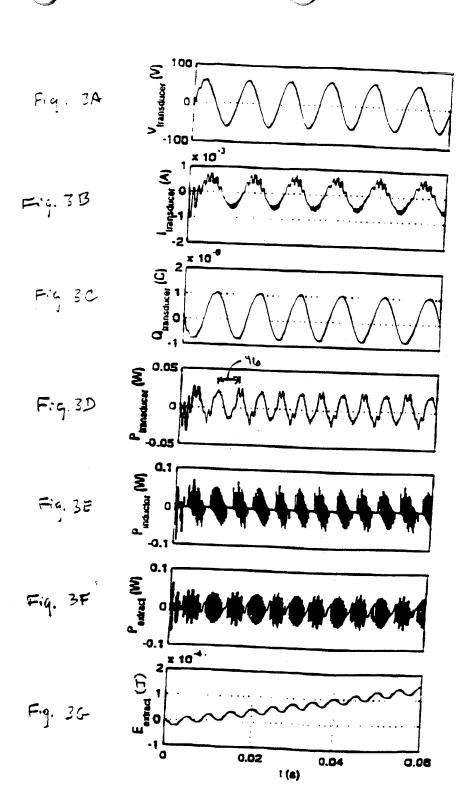
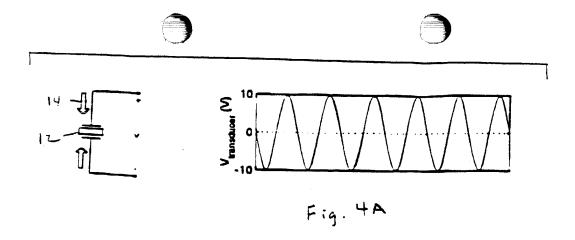


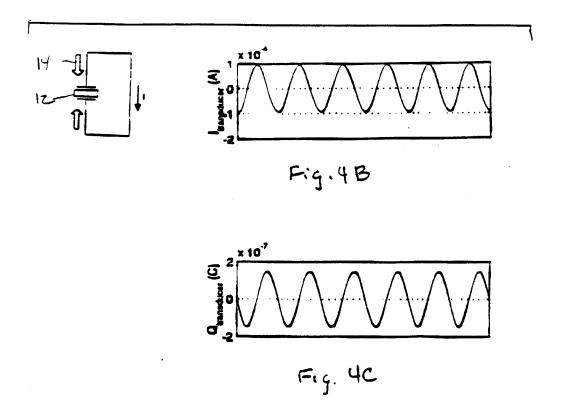
Fig. 2A

Fig ZB





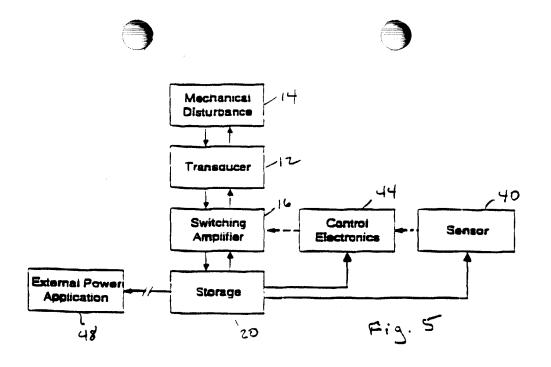


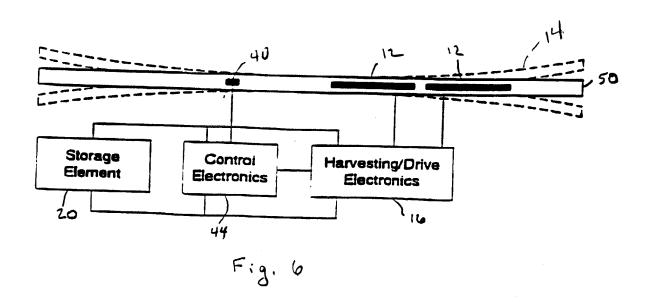


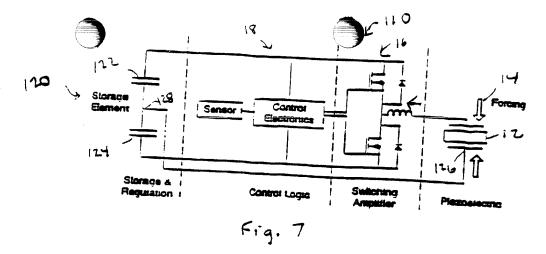
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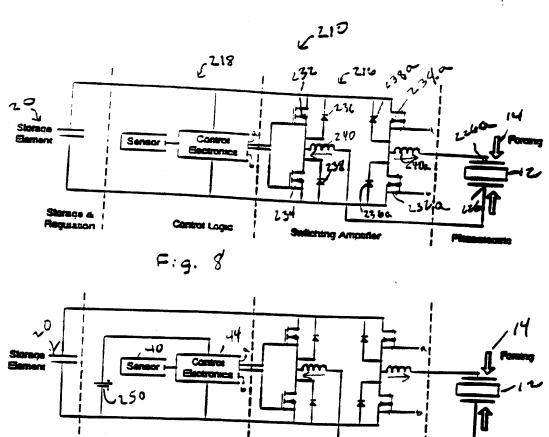


Fig. 9

Control Logic

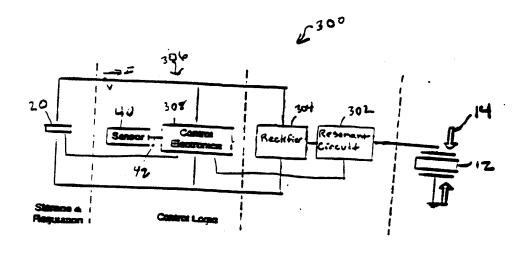
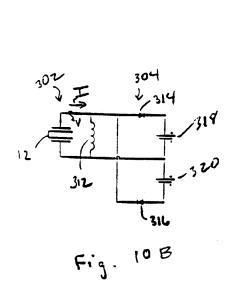
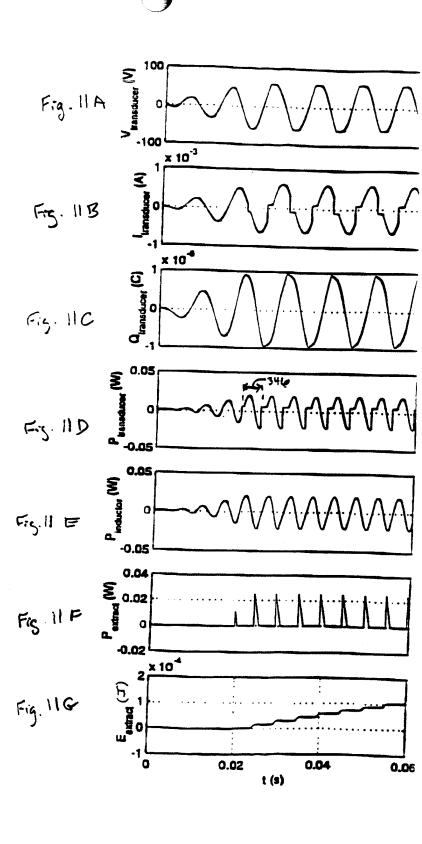
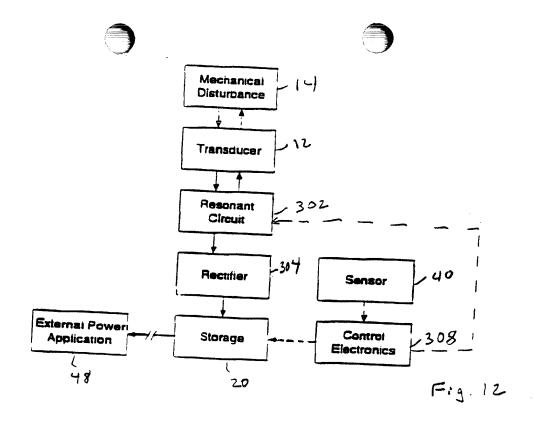
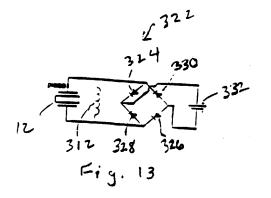


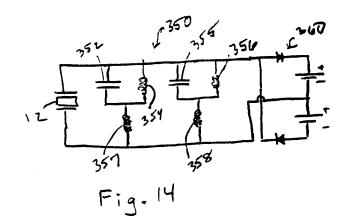
Fig. 10 A

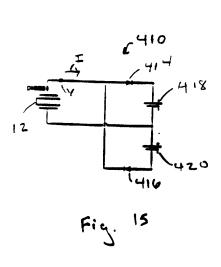


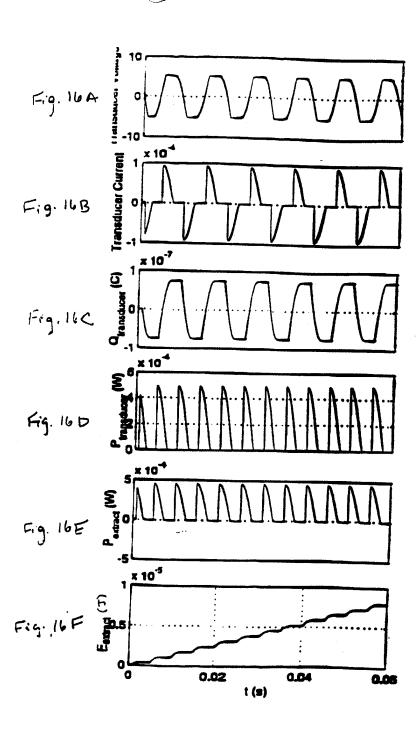












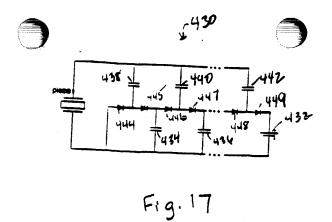




Fig. 18A

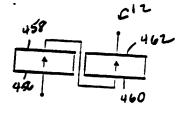
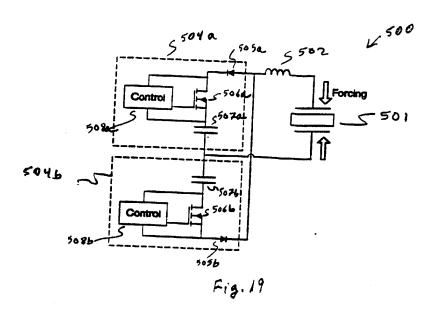
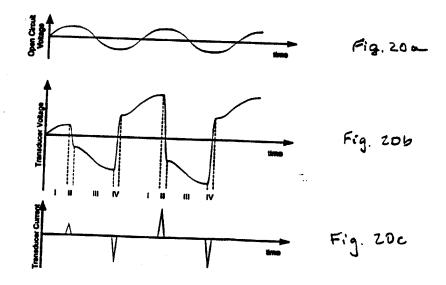


Fig. 18B





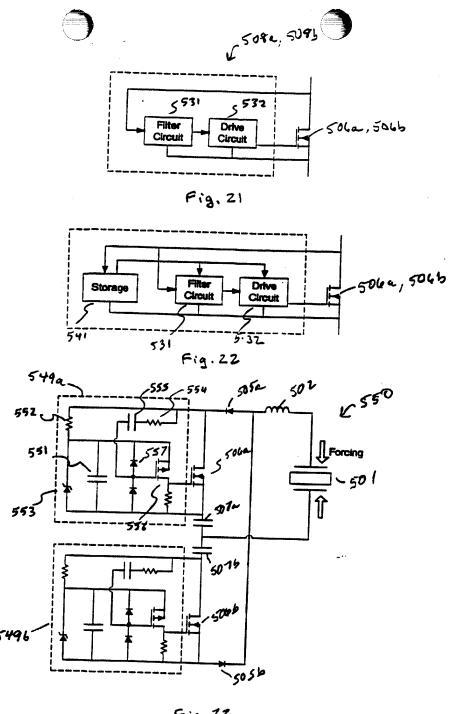
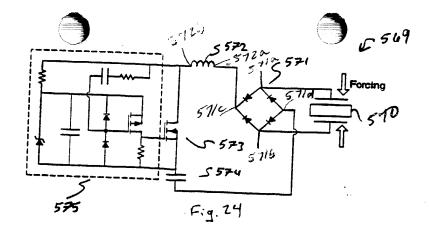
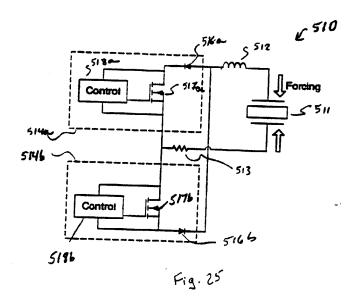
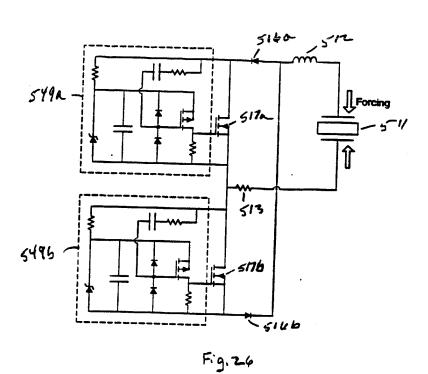
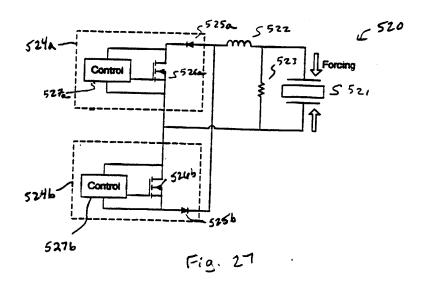


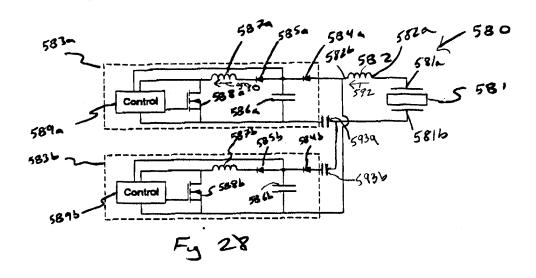
Fig. 23

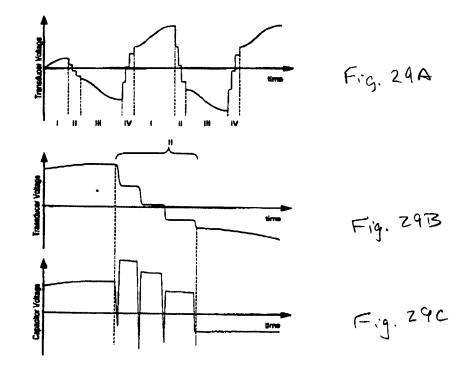












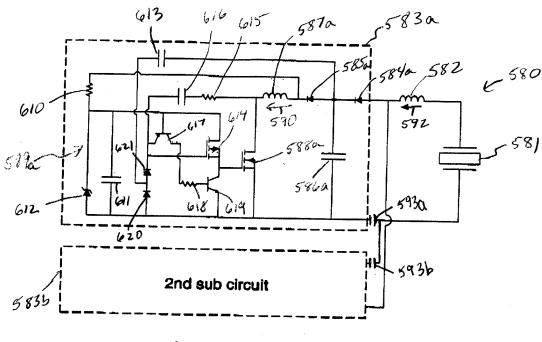


Fig. 30